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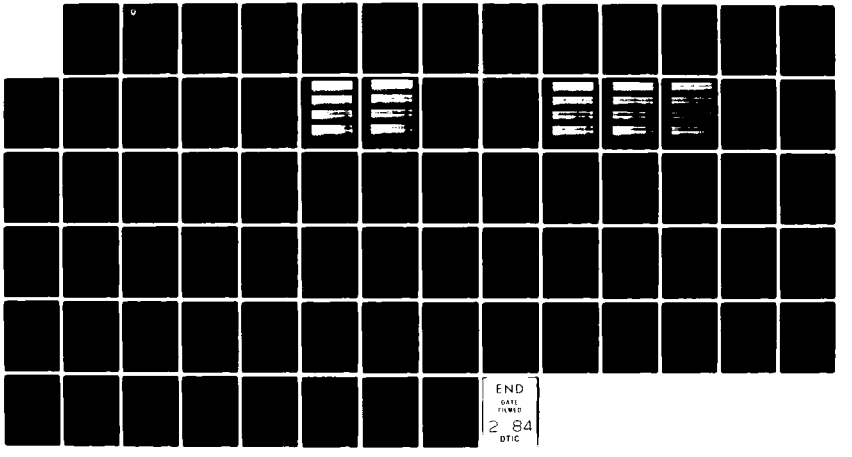

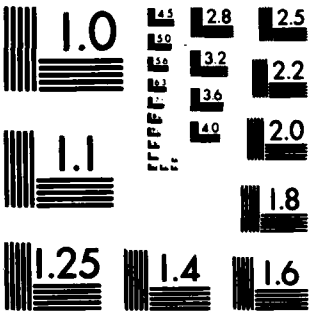

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RESEARCH AND DEVELOPMENT TECHNICAL REPORT
CECOM-80-0520-2

# ARMY DIGITAL TEST REQUIREMENTS REPORT

MANTECH INTERNATIONAL CORPORATION
2320 MILL ROAD
ALEXANDRIA, VIRGINIA 22314

DECEMBER 1983

Final Report for Period Oct 1982 — Dec 1983



PREPARED FOR:
US Army Test, Measurement and Diagnostic
Technology Laboratory



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The advent of digital VLSI circuit design is causing both the capabilities and technology of Army digital prime equipment to rapidly advance. Thus, the testing requirements of this equipment are becoming more complex than they have been in the past. Higher clock and data rates are particular testing requirements that are presenting testing difficulties for existing Army digital testers. The objective of this study is to forecast the impact of this future technology on the TMDE equipment testing requirements for the

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20. Abstract (continued)

1988-1991 time frame. This forecast is based in part on the analysis performed in a previous report entitled "Army Digital Test Requirements Analytic Report". It is anticipated that this forecast will assist the Army in providing needed timely digital ATE support for the Army prime equipment fielded in the 1988-1991 time frame. In addition to the forecast, this report provides specific recommendations concerning stimulus/measurement requirements and test program development techniques to support future Army prime equipment.

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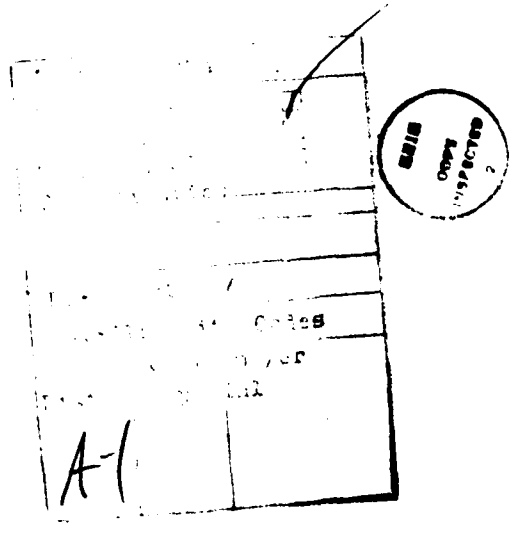


## EXECUTIVE SUMMARY

This report is the second part of a two part report which documents the results of efforts undertaken from October 1982 to October 1983 to project and quantify the Army digital testing requirements for the 1988-1991 time frame and describe functionally the digital ATE characteristics/attributes required to meet these testing requirements. The first part of this report entitled "Army Digital Test Requirements Analytic Report" describes the methodology utilized to conduct the study and provides a summary of the digital technology studied in detail.

Study efforts conducted on behalf of this project dramatically indicate that digital technology is rapidly advancing. A primary/major finding of this report is that trend analysis of the data collected indicates that the newer digital technologies are demanding faster speeds (dynamic testing), longer test patterns (sequential testing) and greater accuracies to be properly tested and are outpacing the functional capabilities of existing fielded Army ATE.

A summary of the projected digital test requirements and ATE characteristics for the 1988-1991 time frame are presented in Table 4-1 and 5-1 respectively, in this report.

A second finding is that the existing inventory of military and commercial digital equipment present so many major variations and combinations of digital test requirements that it has become a difficult if not an impossible task to select one particular cost effective digital tester design to satisfy all of the present and future Army testing needs, some of which may not yet be determinable. Thus, it has been a finding of this report that the only feasible approach to cost effective digital ATE design is one that continues to provide the necessary modularity and flexible testing capabilities which enable a generic design approach that is both reconfigurable and tailorable. This approach can best meet the ever changing Army digital testing requirements in the most cost effective and technically responsive manner because it allows the Army to make new technology insertions in their digital ATE testers.

As for the need of further studies identified in the report, the following two recommendations are made:

- The Army should investigate and identify the problems in the development and design of a ATE interface that can handle up to 100MHz signals which will be required for testing future high speed VLSI and VHSIC chip populated PCBs.

- The Army should investigate/study the possibility of enhancing ATPG's by marrying ATPG algorithm systems with artificial intelligence and parallel processing techniques.

## 1.0 INTRODUCTION

### 1.1 BACKGROUND

The advent of 8-16 bit microprocessor-based digital circuit boards which operate at 1-10 MHz in current Army weapon systems has strained existing Army ATE assets. Testing and fault-diagnosing these microprocessor-based sytems with present Army ATE requires excessive testing times and expensive interface adaptors to handle bidirectional data and high-speed data rates. Existing Army Automatic Test Program Generators (ATPGs) are not capable of developing test patterns for most of the microprocessor-based circuit boards, thus straining the Army Test Program Developers. This, in turn, increases Test Program development costs since manual pattern generation techniques are required.

To complicate the situation even further, new (1988-1991 time frame or beyond) Army weapon systems are likely to incorporate the following technologies:

- o 1-3V Low Voltage Logic Families
- o 32 BIT or Greater Bidirectional Data Bus
- o Memory Chips of 1 Megabit
- o Dynamic VSLI Chips operating at frequencies up to 100MHz
- o Special functional chips as digital filters, digital correlators, etc.

The above technology advances will widen further the gap between existing Army ATE system testing capabilities and prime equipment testing requirements. Thus, TMDE has taken such measures as the funding of this study so that it can assist the Army in meeting the high-technology challenge and can obtain for its inventory digital Automatic Test Equipment and diagnostic software aids capable of handling the testing requirements of tommorrow's technology.

### 1.2 OBJECTIVE

The objective of this report, which is the follow-on report to the "Army Digital Test Requirements Analytic Report", is to assist the Army in meeting the challenge of defining the scope of the digital testing requirements for the 1988-1991 time frame and determining future digital ATE characteristics. Thus, the Army can direct advanced

digital test technology R&D efforts and develop a technical specification for acquiring the next generation Army digital ATE system.

## 1.3 REPORT ORGANIZATION

The remainder of this report is organized into sections (2 through 6) that provide mainly overviews/recommendations and appendices for detailed discussions, bibliographies and acronyms/abbreviations. A brief description of sections 2 through 6 and appendices is provided below:

- **Section 2** - identifies the generic categories and digital electronic equipment studied in detail for this report.

- **Section 3** - summarizes and depicts in graphic form the results of the digital technology projection efforts.

- **Section 4** - discusses the digital testing requirements for the 1988-1991 time frame based on the "Army Digital Test Requirements Analytic Report," ATE industrial survey, and digital technology projection of section 3. The results are then presented in table form for ready reference.

- **Section 5** - discusses the projected ATE characteristics and requirements and manifests them with corresponding characteristics of contemporary VLSI ATE and presents primary Army generic ATE.

- **Section 6** - discusses manual pattern generation and simulator/automatic test program generation. Also, conclusion/recommendations regarding ATPG enhancement are provided that would improve future TPS development.

Appendix A presents the considerations for selection of ATPG tools. Appendix B lists the reference material used in the preparation of this report. Appendix C provides the explanation for acronyms/abbreviations used.

## 1.4 METHODOLOGY

In order to meet this objective, this report has used the methods and results of the analytic approach described in the "Army Digital Test Requirements Analytic Report" to formulate the following:

- Digital Technology Projections
- Digital DUT Test Requirements Projections
- Digital ATE Requirements/Characteristics Projections
- Test Program Set Generation Technique Discussions/Recommendations

## 2.0 SCOPE

In this report, the principle time frame used for the digital technology/test requirements projections is 1988 through 1991.

The generic categories of equipment considered during this study were:

- o Communications Systems
- o Weapon Systems
- o Avionics Systems
- o Military Computers
- o Commercial Microcomputer/Memory Systems

Within each equipment category, representative types of equipment were considered in detail. The size of the study, together with the range of equipment being considered, dictated that representative equipments within each equipment category be studied in depth and the test equipment requirements of these equipments serve as the requirements for the entire category. The representative equipment types were chosen as described in the "Army Digital Test Requirements Analytic Report." The selected digital equipment is listed in Table 2-1.

For further details regarding the scope of this report refer to the "Army Digital Test Requirements Analytic Report."

Table 2-1. Generic Categories of Equipment Studied

| Communications Systems | Weapon Systems | Avionics Systems | Military Computer Family | Commercial Microcomputer/Memory Systems |
|---|---|---|---|---|
| AN/PSG-2A | PATRIOT | AN/AYK-14 | AN/UYK-41 | Intel Single Board Computers |
| CP-1406/TYQ | MLRS | | AN/UYK-49 | Intel Bubble Memory |
| Multiplexer TD-1236 | XM-22 | | Single Module Computer | Intel 64K RAM |
| | | | | Intel DMA Controller |
| | | | | Intel Intelligent Communications Controller |
| | | | | IBM Disk Memory Set |

## 3.0 DIGITAL TECHNOLOGY PROJECTIONS

### 3.1 TECHNOLOGY AREAS INVESTIGATED

There are, at present, ten different semiconductor digital device technologies in widespread use. In addition, one (1) new technology is beginning to yield usable devices, while one other is still in the R&D category. The twelve circuit technologies are the following:

- o Current Technologies
  - A. Bipolar Devices
    - TTL
    - Schottky TTL
    - Integrated Injection Logic ($I^2L$)
    - ECL
  - B. MOS Devices
    - PMOS
    - NMOS
    - Bulk CMOS
    - CMOS/SOS
  - C. Integrated Schottky Logic (ISL)
  - D. Schottky Transistor Logic (STL)
- o Developmental Technologies (13, 14)
  - A. Gallium Arsenide (GaAs)
- o R&D Technology
  - A. Josephson Junction

Table 3-1. Summary of IC Technology Characteristics

| PROPERTIES | CURRENT IC TECHNOLOGIES | | | | | | | | | | DEVELOPMENTAL |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | $T^2L$ | $LST^2L$ | ECL | $I^2L$ | PMOS | NMOS | BULK CMOS | CMOS/SOS | ISL | STL | GaAs |
| Propagation Delay, ns (typical value) | 6 to 30 (10) | 2 to 10 (5) | 0.3 to 2 (2) | 7 to 50 (20) | 30 to 200 (100) | 4 to 25 (15) | 10 to 35 (20) | 4 to 20 (10) | 1 to 2 | 1 to 2 | .05 to 0.1 |
| Speed-Power Product (pJ) | 30 to 150 | 10 to 60 | 15 to 80 | 0.2 to 2.0 | 50 to 500 | 5 to 50 | 2 to 40 | 0.5 to 30 | N/A | N/A | 0.01 to 01 |
| Typical Supply Voltages (volts) | +5.0 | +5.0 | -5.2 | +0.8 to +1.0 | -15 to +20 | +5.0 | +10.0 | +10.0 | +5 | +5 | +1.2 |
| Signal Swing (volts) | 0.2 to 3.4 | 0.2 to 3.4 | -0.8 to -1.7 | 0.2 to 0.8 | 0.0 to -15.0 | 0.2 to 3.4 | 0.0 to 10.0 | 0.0 to 10.0 | N/A | N/A | 0.0 to 0.8 |

NOTE: Table 3-1 is based on data from references (10), (11), (13), (14), (16), (18), (21), and (33).

The comparative properties of these technologies, with the exception of Josephson Junction, are enumerated in Table 3-1. It is ManTech's professional opinion after investigating Josephson Junction technology that it will not be factor in military equipment other than as applied to supercomputers because of its super cooling requirements. From Table 3-1 it appears that, based on propagation delay and speed-power product, the technologies which are likely to be dominant in the 1990s are GaAs, CMOS/SOS and possibly ECL. It also appears that power supply voltages will be lower than the current standard, +5V. (22)

In addition to the foregoing commercial areas of technology, the Department of Defense's Very High Speed Integrated Circuits (VHSIC) Program was also investigated (37). This effort is being performed by six contractors and is employing the following technologies:

- o Bipolar Devices
  - A. ISL
  - B. STL
  - C. Triple Diffused TTL
- o MOS Devices
  - A. CMOS/SOS
  - B. NMOS
  - C. Bulk CMOS

Phase I of the program (1980-1984) is initially aimed at achieving the following goals:

- o Higher resolution chip layout - 1.25 micrometers
- o Higher densities - to 1000 gates/$mm^2$
- o Speed-density products - to 5 X $10^n$ gate-Hz/$cm^2$
- o Lower power dissipation - to 2 uW/gate

By the end of Phase II, chip resolution layout will be of the order of 0.5 to 0.8 micrometers, which will enable circuits on a 1 $cm^2$ chip and containing over 100,000 gates to function at clock rates of 100 MHZ.

To date, the VHSIC Program has announced the development of two devices (29, 38), namely, a 25 MHZ matrix switch device and a 80 MHZ digital correlator. Further developments are expected to be announced as Phase I nears completion. Bid submission for Phase II has recently begun.

A parallel DOD program to develop U.S. sources of Gallium Arsenide memories and gate arrays was recently announced (34), but no technical goals have yet been established.

Data was also obtained on the Military Computer Family (MCF) program. Preliminary specifications for the MCF program include a target clock frequency (for the AN/UYK-41 Super minicomputer) on the order of 25 MHz and an I/O data rate of 6 megabytes/second with a 32 bit word length. The technology to be employed in the MCF program has not yet been selected. MCF production is expected to start in 1987.

## 3.2 DIGITAL TECHNOLOGY TRENDS

The interpretations and conclusions on the future of digital technology which follow are based on the results of the ATE industry survey, the study of commercial and military technical literature and related studies made by ManTech.

Figure 3-1 depicts the growth in dynamic and static semiconductor RAMs since 1970. The pattern is for DRAM bit density to quadruple every 3 years, with static RAMs following about 3 years behind. This pattern is expected to continue, producing, in the 1988-1991 time period, DRAMs of 4 to 16 Mbits/chip and static RAMs of 1 to 4 Mbits/chip.

Figure 3-2 plots the technology trends from 1972 to the present to depict the ever decreasing access times for various sizes of dynamic and static RAMs for four (4) technologies, namely, NMOS, CMOS, ECL and GaAs. Any specific accurate projections

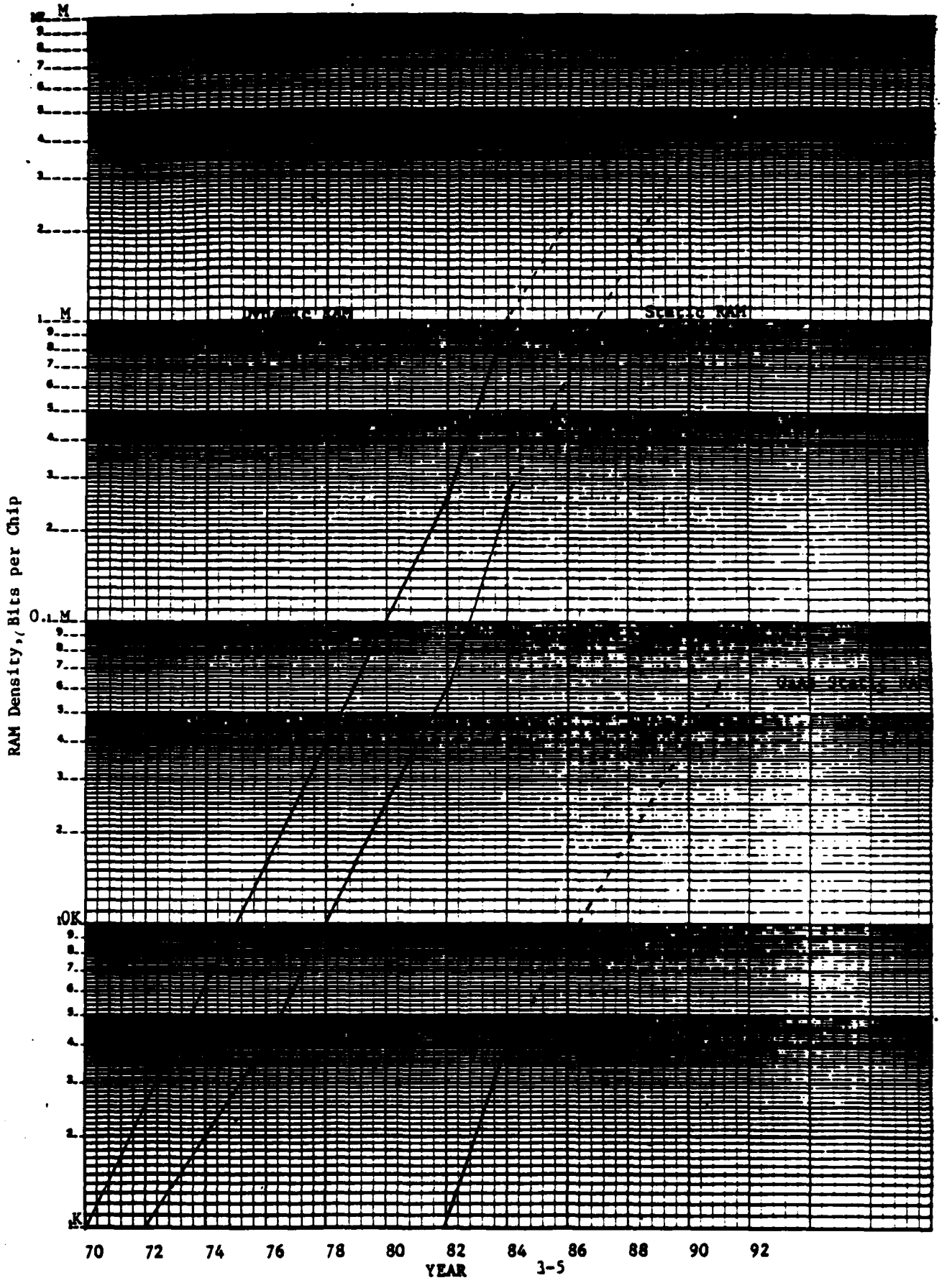



Figure 3-1. Trend Curves for RAM Density

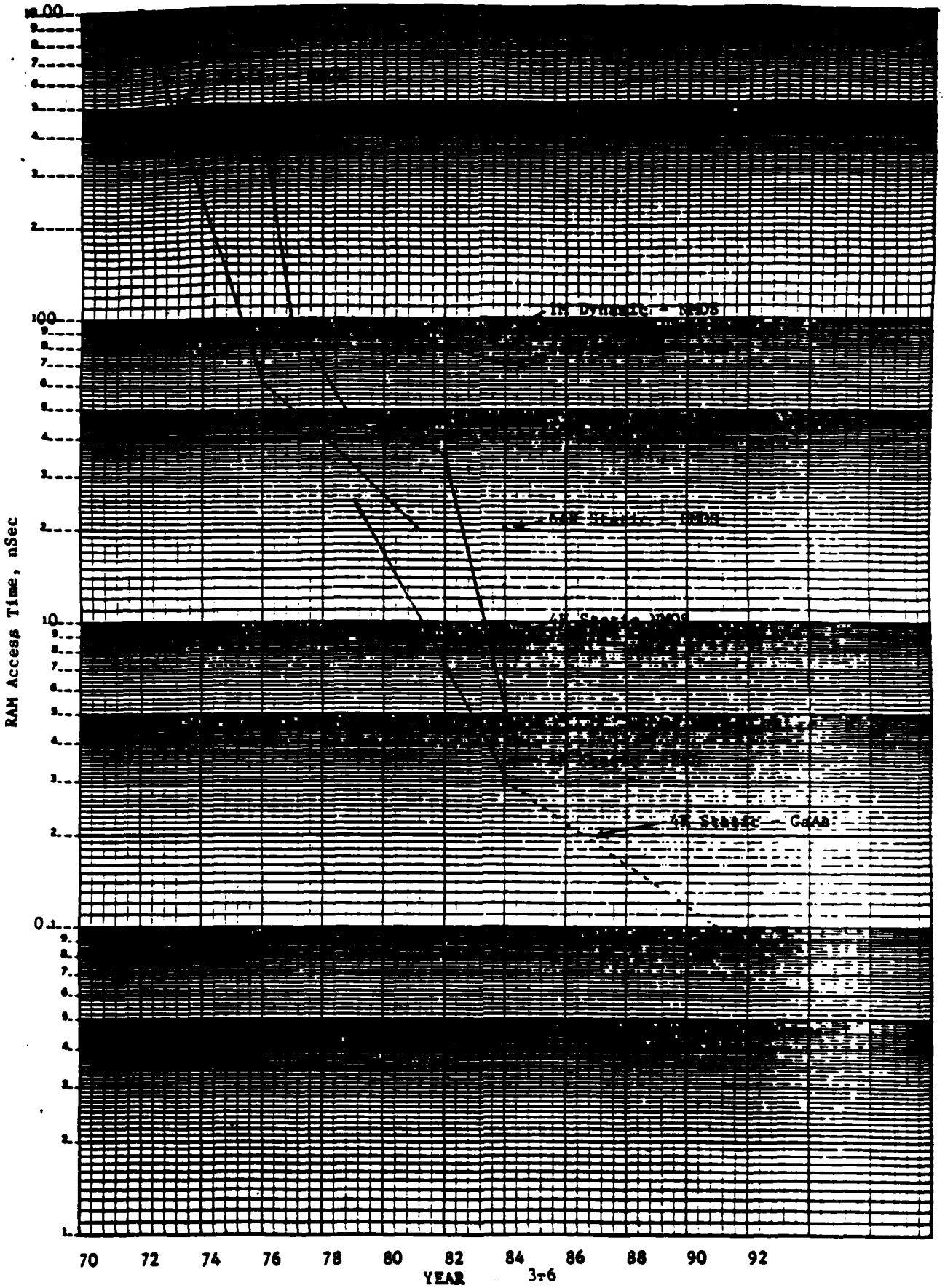



Figure 3-2. Trend Curves for RAM Access Time

of future access time for all these categories for the 1988-1991 time frame were found to be impossible from the data available. However, based upon previous history and the present amount of research and development being performed by industry today, it is expected that RAM access time for all memory sizes will decrease in the future. Most likely the 4K GaAs static RAMs will have access time below 1 nSec. Note that PCBs containing such large fast RAMs will require testers to supply large volumes of data at a fast rate in order to hold memory board test time to a reasonably figure in the future.

Figures 3-3, 3-4 and 3-5 show the progress of microprocessor word length, clock frequency and instruction cycle time since 1970. Word length, which increased from 4 bits in 1971 to 32 bits in 1982, is expected to reach 64 bits in the 1988-1991 period. Clock frequencies are expected to be in the range of 60 to 100 MHz in that period with instruction cycle times on the order of 20 to 100 nSec for state of the art microprocessors. The effects of Gallium Arsenide on microprocessor progress are not projected since no GaAs processor has yet been developed.

## 3.3 CONCLUSIONS

The pace of technological progress in the 1988-1991 time frame promises to be rapid. The present lag between military and commercial use of new technology has been estimated at as much as ten (10) years of longer (37). However, with the advent of such programs as the Military Computer Family (MCF) and VHSIC such military "technology insertion gap" should be greatly reduced.

Thus, by 1991, the changes in Army electronic equipment technology will be substantial and the equipment technology will be more in pace with its contemporary commercial technology than they are today. The VHSIC and MCF programs will be producing hardware for deployment, with clock rates in the 25 to 100 MHz range. Higher speed military data buses (in order of 20 Mb/s depending on technology available) will be used instead of the MIL-STD-1553 bus (1 Mb/s) (28). Commercially, gigahertz logic, based on GaAs technology, is anticipated, with memory access times under a nanosecond and throughput rates approaching 1 billion floating point operations per second. Dynamic RAMs are expected to reach densities between 1 and 10 million bits per chip.

The IC technologies expected to be encountered in Army digital fielded or developmental electronic equipment are TTL, Schottly TTL, $I^2L$, ECL, PMOS, NMOS, CMOS, CMOS/SOS and perhaps GaAs. Gallium Arsenide technology might start appearing in Army computers in the area of Arthmetic Logic Units (ALUs) and cache memories.

It thus appears that, as a minimum, the Army's microprocessor based system technology of equipment fielded 5 to 8 years from now will consist for the most of IC technology in Table 3-1, contemporary and 1988-1991 time frame commercial ICs and VHSIC program developed ICs. This means that the primary digital performance characteristics for Army microprocessor based equipment in all likelihood will have the following range of values:

| | |
|---|---|
| Clock Frequencies | 1 to 100 MHz |
| Data Rates | .01 to 10 megabytes |
| Word Length | 8 to 64 bits. |

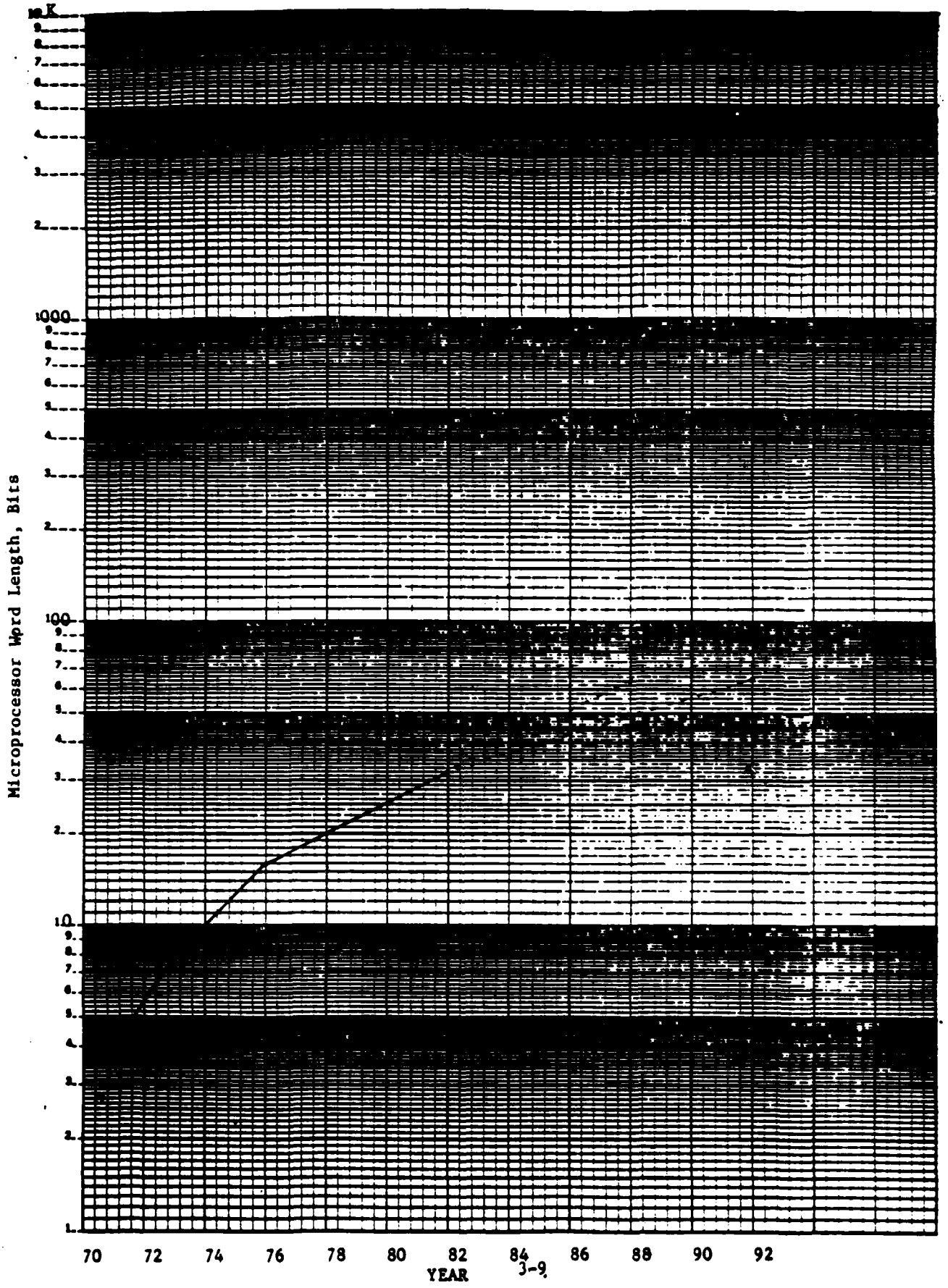



Figure 3-3. Trend Curves for MP Word Length

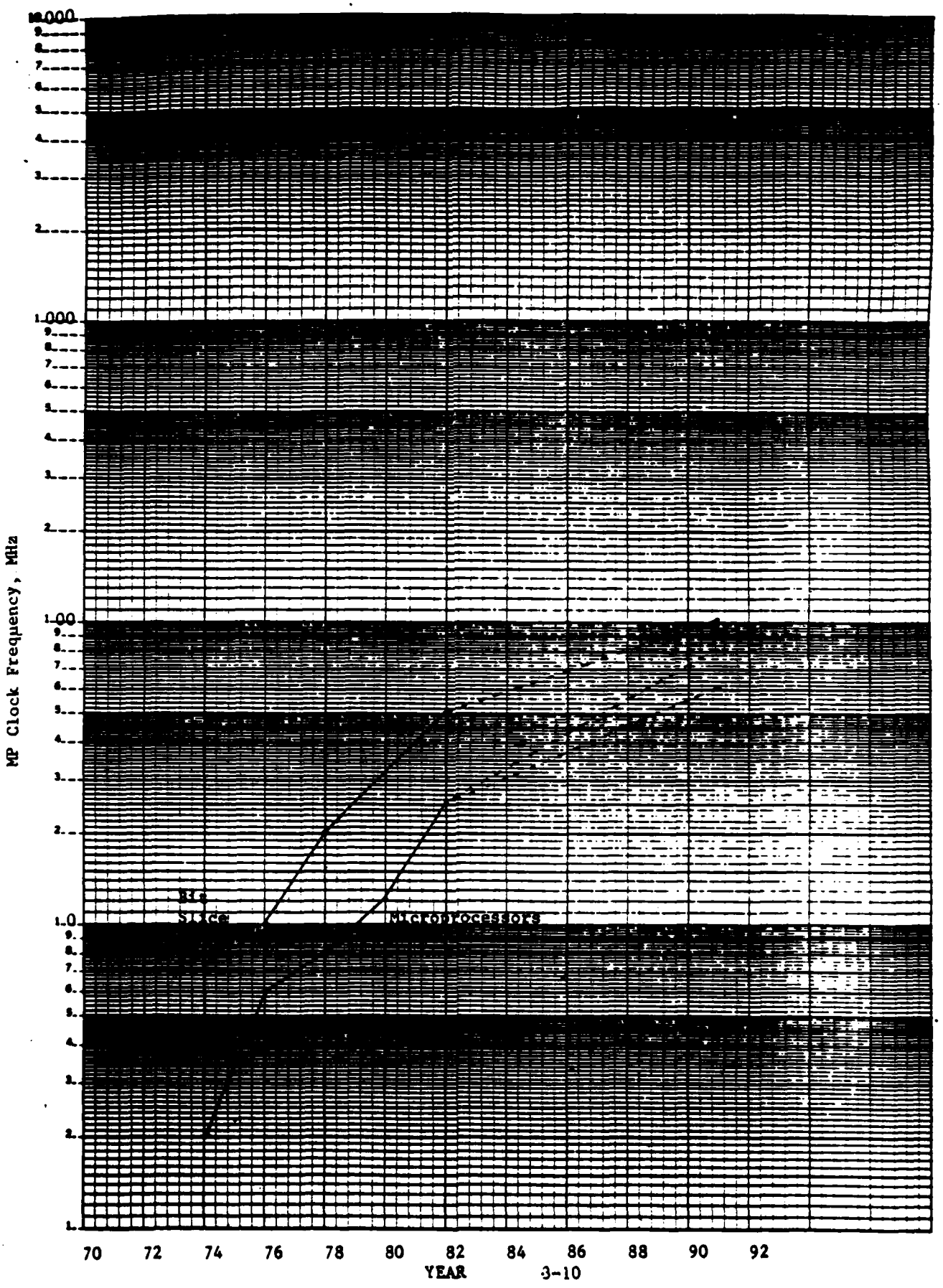



Figure 3-4. Trend Curves for MP Clock Frequency

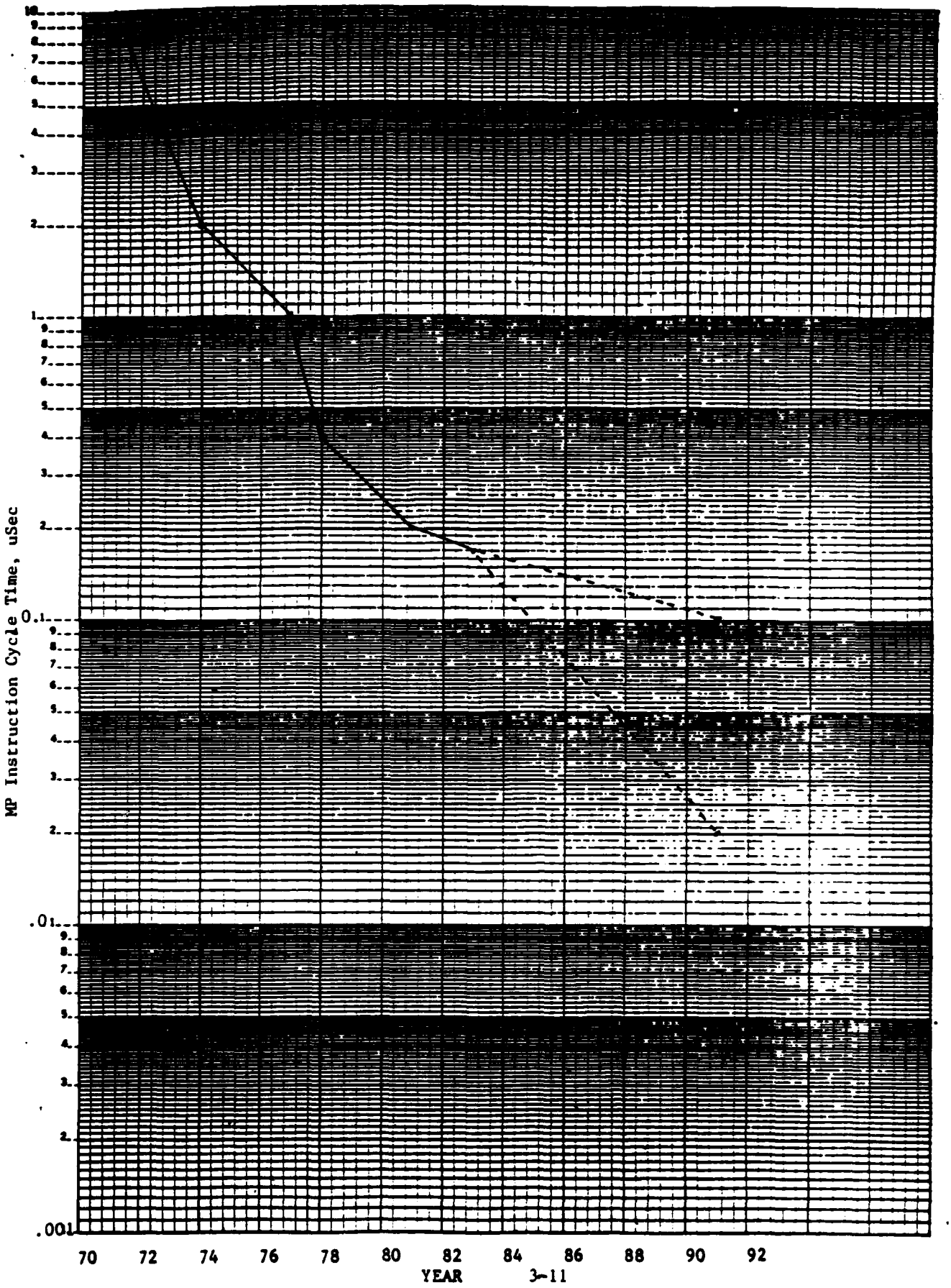



Figure 3-5. Trend Curves for MP Instruction Cycle Time

# 4.0 DIGITAL DUT TEST REQUIREMENTS PROJECTIONS

## 4.1 INTRODUCTION

This section discusses the digital stimulus and measurement capabilities that will be required to maintain the Army's digital prime system in the 1988 - 1991 timeframe. These capabilities will generally be required regardless of the maintenance support level at which the equipment is employed. Also, closely related to these projected test requirements, it should be noted that the Army has recognized the need for Design for Testability (DFT) features to be designed into the prime equiment during the development process because DFT can affect the testing complexity of the Device Under Test (DUT). Consequently, the Army has required that all new Army weapons be designed in accordance with proposed Military Standard XXXX, dated 24 January 1983 and entitled "Testability Programs for Electronic Systems and Equipment." This standard includes all the Army testability requirements for built-in test (BIT) and ATE off-line testing. Army systems fielded prior to this requirement will have some design for testability or practically none at all. In either case, they must be tested by ATE.

## 4.2 FUTURE DIGITAL TESTING REQUIREMENTS

### 4.2.1 INTRODUCTION

Based on the literature researched (see bibliography, Appendix B) and the industrial survey, rapid advances in the state-of-the-art of digital integrated circuits technology are being made and are expected to continue. The advances will continue to result in denser VLSI chips, smaller module packaging, more complex circuits and denser printed circuit boards. Predictably, these advances will also result in fewer available circuit test points and more bus-oriented circuit in the post 1988 digital printed circuit boards. However, the parametric data available for fault detection and isolation of digital logic circuits in the post-1988 era is expected to involve, as it does today, the following:

- Circuit board test patterns
- Clock rates
- Circuit board input/output currents and voltages
- Switching speeds/rise and fall times/data rates
- IC pin voltages and currents

- o IC pin test patterns
- o Accessible test points.

Consequently, future performance and fault isolation procedures using these parameters will continue to require ATE support for supplying the required stimulus, measuring the response and isolating the faulty components, for the same reasons as they do today. Namely, the test procedures using these parameters will be time consuming and tedious if manual techniques are used. In addition, any manual testing would require highly trained operators of which there is a shortage in the military.

However, even though the testing of digital equipment will continue to largely require the capability to generate a sequence of digital test patterns at proper current and voltage levels to stimulate the device under test, monitor the output pattern response and compare with expected response patterns, this investigation's findings clearly indicate that state-of-the-art and future digital technology will make test requirements more stringent than they are today.

### 4.2.2 GENERAL TEST REQUIREMENTS

Generally, the digital tester will be required to operate in the static and/or dynamic modes in order to support the new technology, the older existing technology and the technology presently being supported on the USM-410 for the reasons given below:

- o Static Mode

  Existing digital technology generally was tested in the static mode and for program transportability reasons this is still required. Also, even the newer digital technology can in many incidences instances be checked best statically particularly when looking for hard faults or when performing some simple fault isolation test.

  In static mode, a single digital pattern is used to stimulate the DUT, the circuit responds, and the output is compared to the correct response. If the response is incorrect, the response pattern is analyzed to determine the possible faulty card/IC. Then, a new stimulus pattern is applied or manual

probing or a combination of both techniques is used to isolate the faulty card/IC. Throughout this procedure, the digital circuitry is being operated at a rate far below that at which the circuitry normally operates, hence the name static testing.

Two of the main criticisms of static testing are that it does not truly test the operational capabilities of the circuitry under test and that it can produce excessively long test times particularly with complex systems/boards where a large number of digital test patterns are required, namely, in the thousands.

- Dynamic Mode

With the advent of new dynamic VLSI (i.e., microprocessors) which must be operated within a specified range of clock frequencies in order to function, digital stimuli must be provided to the board during testing with rates well above the kilohertz range, with clocks generated either by the tester or by the board under test. In addition, the interface between the tester and the board is usually a bi-directional bus, and the tester driver/sensor pins may be required to switch between inputs and outputs at high speed so that the board can provide data output on the bus on clock cycle after the tester has provided the instruction input on the same bus. In other words, the board tester should have the capability to look more and more like the system environment, operating at full system operating rate, or even faster, to capture marginal faults.

Also, the bus structure of most VLSI boards is a result of the partitioning of the circuit functions by the VLSI chip designers. It makes the circuit board designer's task easier because the interface between the VLSI chips is well-defined. However, it makes fault isolation more difficult because of the many devices on the same bus, any of which could cause the fault. Fault isolation is also made more difficult because the traditional static stuck-at-one or stuck-at-zero fault is less accurate for VLSI boards since failure modes can include timing problems, dynamic failures, and "soft" failures such as data sensitivity and device interaction. Thus a functional tester operating at full speed is needed to detect these subtle failure modes.

Furthermore, the fault detection process will continue to become more and more complicated with the growth of usage of very large scale integrated devices/microprocessors and associated complex bus structures in military systems. Consequently, dynamic testing must be performed through these busses in a timely and accurate manner.

### 4.2.3 SPECIFIC TEST REQUIREMENTS

The key projected test requirements parameters for the 1988-1991 timeframe are summarized in Table 4-1. These projections are consistent with the idea that the capabilities of the tester should at least be commensurate with the technology of the equipment to be tested. The technology of the equipment to be tested and the basis for test requirement projections were presented in section 3.0 of this report and the "Army Digital Test Requriements Analytic Report." These projected test requirements are used as a basis for predicting the required future ATE input/output characteristics in section 5.0. Specifically, the projected figures in Table 4-1 were obtained as follows:

- I/O Pin Count: Army data base 38 to 256; projected to be 512 max.

  This projection is based upon the premise that the majority of current VLSI ATE testers do not exceed this max I/O pin count and are able to accommodate the testing of PCBs containing VLSI chips.

- Max Vector Pattern Rate: Army data base 2MHz; projected to be 100MHz

  This pattern rate will be necessary to test PCBs containing VLSI and VHSIC chips. In the analytic report commercial clock rates for such PCBs were reported as high as 200MHz. The MCF will have a clock rate in the order of 25MHz and VHSIC has developed digital correlated operating at 80MHz. Also, there are commercial testers for VLSI chips operate at 100MHz.

- Max Vector Pattern Depth: Army data base 32K patterns; projected to be 1M patterns

  This vector pattern depth will be required for testing microprocessor based PCBs having a 32 to 64 bit data bus, MCF memories, PCBs of 8 megabytes, and from projection of commercial data base PCBs with memories of 16 megabytes, and PCBs containing many VLSI chips.

- "MAX Data Skew": Army data base 30 nsec; projected to be 0.5 nsec.

  This max data skew is required for the 100MHz vector pattern rate.

- Max Clock Rate: Army data base 9MHz; projected to be 100MHz

  This is required for the same reason that the max vector pattern rate of 100 MHz was required.

- Max Source/Sink Current: Army data base 50 ma; projected to be 100 ma

  This max source/sink curent is required to enable the driving of 50 ohm terminations during testing.

- Max Number of Logic Family Types Tested Simultaneously: Army data base 3 types; projected to be 3 types

- Programmable Logic voltage Level Swing: Army data base -18 to 28V; projected $\pm$15V for dynamic testing and $\pm$ 30 V for static testing.

  Reference Table 3-1, all the dynamic current developmental IC technologies operate with logic swings between -15V and +15V. Signals outside the $\pm$15V range are usually static signals.

- Minimum Programmable logic Level Resolution: Army data base ±50 mV; project requirement is ±10mV

This is based on the project that future logic level swing will be smaller because of lower operating voltage and the ICs.

**Table 4-1**

**Summary of the Key I/O Digital Test Requirements Projections for 1988 - 1991 Time Frame**

| Parameter | Project Values |
|---|---|
| Max I/O Pin Count | 512 |
| Max Vector Pattern Test Rate | 100MHz |
| Max Vector Pattern Depth | 1 million vector patterns |
| Max Data Skew | 0.5 nSec |
| Max Clock Rate | 100MHz |
| Max Source/Sink Current | 100 ma |
| Max Number of Logic Family Types Tested Simultaneously | 3 types |
| Programmable Logic Voltage Level Swing | ± 15V dynamic testing<br>± 30V static testing |
| Minimum Programmable Logic Level Resolution | ± 10 mv |

## 4.3 CONCLUSION/RECOMMENDATION

The Army should investigate and identify the problems in the development and design of a ATE tester interface that can handle up to 100 MHz signals which will be required for testing future high speed VLSI and VHSIC chip populated PCBs.

## 5.0 DIGITAL ATE TEST REQUIREMENTS/CHARACTERISTICS PROJECTIONS

### 5.1 INTRODUCTION

In this section, the projected digital ATE test characteristics are based on the following: the data collected and analyzed (reference Tables 2-1 and 3-1) in the preceeding report entitled "Army Digital Test Requirements Analytic Report," section 3.0 and 4.0 of this report and our ATE experience and professional judgement. In addition, in order to provide some measure of comparability between existing digital ATE characteristics and the projected digital ATE characteristics, the characteristics of both projected and existing commercial VLSI and present primary Army ATEs are presented side by side for ready reference.

Generally, the resultant projected ATE characteristics are what is perceived to be the minimum digital ATE capabilities required to handle the testing of the emerging digital technology of the 1988 - 1991 time frame.

### 5.2 TESTING CAPABILITIES

One of the most important attributes of the future military Digital Tester will be its flexibility. Problems usually arise as a result of the rapid growth and advancement of the digital technology that the Digital Test is expected to support. The latest technologies are demanding faster data rate, lengthier test patterns and greater accuracies. With these rapid variations and combinations of digital test requirements it has become nearly an impossible task to satisfy all the present and future needs, which may yet not be determined, in one tester configuration.

The projected ATE characteristics considered and their required capabilities for the future Army Digital testers are described below:

- o I/O Pins

  Most modern military ATE systems under development are being developed under "Modular" concept where the ATE testing resources are reconfigurable to meet the testing requirements for all the UUTs of a particular system that

is tested. Thus, although a maximum of 512 I/O pins will be needed in some cases, in many cases a much smaller number of I/O pins is required. In addition, many UUTs need only static testing, while others need dynamic testing. Three types of reconfigurable 64 I/O pins digital modules will satisfy these requirements: (1) a static digital I/O pin module that would have maximum vector pattern rate of a 100 KHz, (2) a medium speed digital I/O module that would have a maximum vector pattern rate of 10 MHz, and (3) a high speed dynamic digital I/O module that would have a maximum vector pattern rate of 100 MHz. These three types of 64 I/O pins digital modules can be configured in an ATE system to provide up to 512 I/O pins to provide the vector pattern rates required for the UUTs of each system. Thus, the ATE would be configured to provide only the digital I/O pins required to test the UUTs of that particular system rather than 512 I/O pins, operating at vector pattern rates of a 100 MHz in order to test the UUTs of all systems. This results in a considerable cost saving.

- Programmable Pins

In order to meet the testing requirements of the variety of IC logic families and bi-directional data busses that will be incorporated in many digital PCBs, each tester I/O pin must be capable of being programmed to be a Driver, a Sensor or Tristated. The Driver high and low voltage levels must be programmable, the Sensor voltage threshold level must be programmable. Each I/O pin must also be programmable such that it can source or sink current when required.

- Tristate Driver/Sensor I/O Pins

Each I/O pin must be capable of being programmed to be a driver or a sensor and the driver must be capable of being programmed to the high impedance state. This is necessary for the testing of bi-directional data busses.

- Vector Pattern Depth

The Vector Pattern Depth is the total number of digital patterns required to test a UUT. A digital pattern consists of logical "ones" and "zeros" whose

width or number cannot exceed the total number of I/O pins. Vector patterns limited to depths of 256 to 4096 existing in older military ATE are much to- low, and are exceeded by many existing commercial systems today, and will not meet the requirements of Army system for the 1991 time frame. The testing of printed circuit boards (PCBs) containing a large number of VLSI chips is going to require test vector patterns as long as 1,000,000 vectors. To determine the ATE requirements for testing VLSI PCB boards, one can look at the capabilities of todays ATE for testing VLSI chips. The majority of these testers have a buffer memory in back of each I/O pin ranging from 4K to 264K. However, by using algorithmic test pattern generators, these testers generate many more vector patterns than the buffer memory capacity and , thus, the buffer memory does not have to reload every time the vector memory pattern exceeds its capacity. The VLSI ATE, with the highest continuous vector memory pattern, is Megatest Corp's MegaOne ATE. This tester can generate 1 million vector patterns at 40 MHz pattern rate to 256 I/O pins. The MegaOne combines one million element vector memory implement in dynamic RAM with a set of four high speed 1K ECL buffers per I/O pin. This is accomplished by interleaving accesses of the dynamic RAM and the small (1K deep) local buffers. By using a unique complex algorithm and the four local buffers per pin, it is possible to make the buffers transparent to the user. Thus, nested loops of any length can be created with the 1 million vectors.

Thus, from the above example, it can be seen it is not necessary to have a large buffer memory behind each pin. Other algorithmic techniques that have been used in ATE testers are algorithmic test pattern compaction, and for memory board testing special algorithmic Memory Pattern Generators (MPG) which automatically generate the data pattern and address patterns for testing high speed memories without requiring a large local buffer memory for every I/O pin.

For testing Army PCBs containing VLSI chips that will exist in the 1991 time, a vector pattern depth of 1,000,000 vector is recommended.

- Programmable I/O Logic Levels

The maximum logic one level, the minimum logic zero level, the maximum and minimum differential voltage between a logic one and a logic zero and the capability for a high impedance state are the major logic voltage characteristics. For these voltage characteristics, the programmable I/O logic levels of ± 15 volts are required for dynamic tesitng and ± 30V for static testing to meet the testing requirement of in section 4.2.3.

- Vector Pattern Rate

In the 1991 time frame, Army digital equipment will require Vector test pattern rates of 100 MHz. Pattern Rate must be fully programmable; that is, operate at a fixed frequency, programmed variable rate, or a rate synchronized to the UUT clock signal.

- Clock Rate

Based on projected UUT digital test requirements of the 1988-1991 time period, a maximum clock rate of 100 MHz is recommended.

- Standard Bus Interface

MIL-STD-1553, IEEE-488 and RS 232C busses are used now and the interfaces should be provided. However, busses operating a high frequency will be needed for Army digital equipment existing in 1991. MCF parallel interface bus has a data rate of 2 megabytes/sec, which is equivalent ot a 16 MHz data rate. The Intel Multibus described in the Analytical Report will operate at 40 MHz (5M words/sec) data rate. These and other interfaces, if deemed appropriate, e.g., frequency of testing requirement, should be added as required.

- Source/Sink Current

Typically, user requirements from the 1.6 ma of sink current needed to drive one TTL load up to 50 ma of source and sink current. However, to drive 50

ohm terminations, it is recommended that 100 ma source/sink current capability be provided for ATE for the 1988 - 1991 time frame

o Max Data Skew

In general, skew is the worst case time difference between the leading edges of any two stimulus bits in a stimulus pattern as they appears at the output. Skew must be much less than the minimum clock pulse width so a figure of 0.5 nanoseconds is recommended for the Army system emerging in the 1988-1991 time frame.

o Response Strobe Delay

This is the time between the clocking out of stimulus pattern and the checking in of the response pattern. Based upon present and 1991 Army requirements, this value should be programmable from 1 nanosecond to 100 millisecond in programmable increments ranging from 1 nanosecond to 100 microsecond depending upon range.

o Number of Simultaneous Logic Family Max

This parameter refers to the number of simultaneuos logic levels the tester can provide. Based upon the findings of part one of this report a maximum mix of three (3) logic levels were encountered.

o Program Logic Level Resolution

Logic levels in future DUTs are projected to be lower than present levels; requiring greater precision in setting, in a resolution of $\pm$ 10 mV will be needed for 1991.

o Clock Outputs

In order to provide the multiphase clock required by many microprocessor-based systems, 4 clock outputs are recommended.

- Probing for Fault Isolation

The ATE should have the capability of computer directed probing to fault isolate a UUT to the circuit node and list the components at that circuit node in order of the component most likely to be responsible for the failure of the UUT. The probing capability must be capable of using the signature analysis technique, the logic state testing with a fault dictionary technique, and a combination of both techniques. The signature analysis technique uses what is known as a Cyclic Redundancy Check (CRC). CRC is accomplished using a group of feedback shift registers and feeding the nodal digital patterns into the input of the feedback shift register and getting a final compressed nodal signature from the output of the feedback shift register. Signatures from the circuit nodes of good UUT are stored in memory, and when a faulty UUT is probed, any nodal signature which does not match the stored signature for a good node, enables the faulty node to be isolated.

The logic state testing with a fault dictionary stores the logic state of each node for a digital pattern that drives a particular fault to the output pin of a UUT. The logic states for the circuit node of a good board are stored in computer memory and when the nodes of a faulty UUT are probed, its logic state at each circuit node is compared to those of the nodes of a good UUT for a particular fault, and thus, the fault can be isolated to a specific circuit node. The disadvantage of logic state testing with a fault dictionary is that it requires much more memory than the probing techniques using signature analysis. The disadvantage of probing using signature analysis is as follows: Signature analysis works with combinational logic, and it works with sequential logic that can be initialized. However, if a fault occurs in a portion of the sequential circuitry that prevents initialization, then probing by signature analysis cannot be used. In this case, a large group of components that could prevent initialization must be called out. However, the capability of using both probing techniques gives one the advantage of having low memory requirements where signature analysis can be used, and a relatively small memory requirement where the logic state, fault dictionary technique is only used for those portions of circuitry where a failure would prevent sequential logic initialization.

The AN/USM-465A uses the signature analysis technique for probing. User's of the AN/USM-465A have also developed an assembly language program that enables the AN/USM-465A digital card tester to use the same probe for the logic state, fault dictionary technique. The AN/USM-410 (EQUATE), ATE uses the logic state, fault dictionary probing technique.

Table 5-1 summarizes the projected digital ATE characteristics above needed to support Army digital equipment for the 1988 - 1991 time frame.

In addition to the capabilities stated in Table 5-1, the digital tester should also provide the following typical operating mode capabilities which are supplied by existing digital test system and have been proven useful:

- o Apply stimulus set N times
- o Stop on first pass
- o Stop on first failure
- o Apply stimulus only
- o Apply stimulus and record response at full test speed
- o Apply stimulus and mask response, then record the result at full test speed
- o Apply N clock then apply stimuli and measure response at test speed
- o Single step
- o External start
- o Start on equal/not equal
- o Pulse detection and measurement
- o Handshake
- o Loop/repeat test pattern, with capability of many larger nester looping
- o Capability to binary increment or decrement a digital vector pattern
- o Capability to binary shift right or shift left a digital vector pattern

## 5.3 CONCLUSIONS/RECOMMENDATION

Based on the data collected and analyzed during the course of this study, the present and future test requirements are ever changing and exceeding the testing capabilities of present military ATE systems. This analysis strongly suggests that, without developing complex interface devices to augment the existing military ATE, there is a need to develop a new more capable Army generic digital ATE tester which

will accommodate the tailorable/configurable design required to meet the ever changing testing requirements.

Therefore, it is recommended that the Army initiate efforts to develop a new generic tailorable/configurable digital ATE tester incorporating projected testing characteristics.

**Table 5-1. Summary of Current vs. Projected ATE Characteristics**

| | CURRENT ATE | | | PROJECTED ATE | |
|---|---|---|---|---|---|
| **Characteristics** | **AN/USM-410 (EQUATE)** | **AN/USM-465A (GR2225)** | **Max Capabilities of VLSI ATE** | **Projected Required Capabilities** | **Notes** |
| I/O Pins | 128 Stimulus Max<br>128 Response Max | 192 | 288 | 64 (min)<br>Expandable<br>to 512 | |
| Programmable Pins | All | All | All | All | |
| Tri-State Driver/ Sensor I/O Pins | N/A | All | All | All | |
| Vector Pattern Depth | 256 | 1024 x 16 | 1M | 1M | |
| Programmable I/O Logic Levels | +20V Drivers<br>±200V Receivers | -12.8 to 12.9V | ±15V | ±15V Dynamic<br>±30V Static | |
| Vector Pattern Rate | 0 to 2 MHz | 0 to 2 MHz | 100 MHz | 100 MHz | |
| Clock Rate | 0 to 2 MHz | 0 to 2 MHz | 100 MHz | 100 MHz | |
| External Clocks (Inputs) | N/S | N/A | 8 | 4 | |
| Standard Bus Interfaces | N/A | 16 BIT $T^2L$<br>0-125 KHz | IEEE-488<br>RS 232 C | MIL-STD-1553<br>RS 232 C<br>IEEE-488 | 1 |
| Source/Sink Current | 100 ma | 5/16 ma | 100 ma | 100 ma | |
| Max Data Skew | 25 nSec<br>Across 128 pins | 200 nSec | 0.5 nSec | 0.5 nSec | |

**Table 5-1. Summary of Current vs. Projected ATE Characteristics (Continued)**

| Characteristics | CURRENT ATE | | | PROJECTED ATE | |
|---|---|---|---|---|---|
| | AN/USM-410 (EQUATE) | AN/USM-465A (GR2225) | Max Capabilities of VLSI ATE | Projected Required Capabilities | Notes |
| Response Strobe Delays | 50 nSec to 1 Sec in 10 to 100 nSec increments depending on range | 50 nSec to 204 uSec in 10 nSec increments | 1 nSec to 0.8 mSec in .1 nSec to 100 nSec increments depending on range | 1 nSec to 100 mSec in .1 nSec to 100 nSec increments depending on range | |
| Number of Simultaneous Logic Family Mix | 1 | 3 | Max to the no. of I/O pins | 3 | |
| Program Logic Level Resolution | + 10 mV + 10V Range ±50mV +10 -50V Range ±500mV ±50 to 200V Range | ±100 mV | ±1.25 mV | ±10 mV ±15V Range ±50mv ±15 to 30V Range | |
| Clock Outputs | N/S | N/A | 8 | 4 | |
| Guided Probe for Fault Isolation | Yes | Yes | Yes | Yes | |
| Level Sensitive Scan Design Pattern Generator | N/S | N/S | Yes | Yes | |

Note 1: Add appropriate busses as required

N/A Not available

N/S Not specified

**Table 5-1. Summary of Current vs. Projected ATE Characteristics (Continued)**

| Characteristics | CURRENT ATE | | | PROJECTED ATE | |
|---|---|---|---|---|---|
| | AN/USM-410 (EQUATE) | AN/USM-465A (GR2225) | Max Capabilities of VLSI ATE | Projected Required Capabilities | Notes |
| Response Strobe Delays | 50 nSec to 1 Sec in 10 to 100 nSec increments depending on range | 50 nSec to 204 uSec in 10 nSec increments | 1 nSec to 0.8 mSec in .1 nSec to 100 nSec increments depending on range | 1 nSec to 100 mSec in .1 nSec to 100 nSec increments depending on range | |
| Number of Simultaneous Logic Family Mix | 1 | 3 | Max to the no. of I/O pins | 3 | |
| Program Logic Level Resolution | + 10 mV + 10V Range ±50mV +10 -50V Range ±500mV ±50 to 200V Range | ±100 mV | ±1.25 mV | ±10 mV ±15V Range ±50mv ±15 to 30V Range | |
| Clock Outputs | N/S | N/A | 8 | 4 | |
| Guided Probe for Fault Isolation | Yes | Yes | Yes | Yes | |
| Level Sensitive Scan Design Pattern Generator | N/S | N/S | Yes | Yes | |

Note 1: Add appropriate busses as required

N/A Not available

N/S Not specified

## 6.0 TEST PROGRAM SET GENERATIONS TECHNIQUES DISCUSSION/RECOMMENDATIONS

### 6.1 INTRODUCTION

The purpose of this section of the report is to discuss considerations and techniques for development of test program sets covering the following areas:

- o Manual Pattern Generation
- o Program Generation Aids

In the following sections, these topics are discussed regarding their advantages and disadvantages as applied to test program set development.

### 6.2 MANUAL TEST PROGRAM GENERATION

Manual test program generation is the process by which a test programmer codes a DUT test without the aid of software tools. The test programmer, possessing some expertise in circuit operations, uses available documentation, in the form of schematics, test specifications and test procedure manuals, to analyze the circuit and generate a test program to test the DUT. To generate the test program the test programmer must develop input stimuli to exercise all the circuit elements. He must also determine what the correct output response of the DUT will be for each given input stimulus.

This method of test program generation is relatively reliable on a simple digital DUT which contains few gates. However, as the complexity of the DUT increases, the test programs become more difficult to generate and the quality becomes heavily dependent on the expertise of the test programmer.

The last phase of manual program generation is the validation of the program. Validation assesses the quality of the test program. To develop a test program, the test programmer must analyze a circuit to develop an input stimuli which will provide a sensitized path to propagate a stuck at "1" a stuck at "0" fault of a circuit element to one or more output pins. An input stimuli which propagates the fault to the output pin of the circuit must be derived for every circuit element. In some cases, the same input stimuli will detect more than one circuit fault.

## 6.3 PROGRAM GENERATION AIDS

### 6.3.1 INTRODUCTION

Existing digital computer software aid generally fall into the two categories listed below:

- o Digital Simulator Based Test Program Generation
- o Digital Automatic Test Program Generators (DATPG)

This section provides a general discussion on their capabilities and advantages/disadvantages. For further information on how to select the proper simulated and DATPG tool, Appendix A provide a detailed discussion on the general selection considerations that should be applied.

### 6.3.2 SIMULATOR BASED TEST PROGRAM GENERATION

A software tool available for test programming is the simulator. Simulator-based test program generation is the process in which programs are produced using a computer model for the DUT circuit in lieu of the actual printed circuit board. In simulator-based generation, the test programmer supplies the input digital stimuli pattern for testing the DUT to the simulator, and the simulator determines how many faults these stimuli pattern detect, and which faults are still undetected.

To generate a test program using a simulator, the test programmer must first provide an exact model of the DUT to the simulation system. This requires the test programmer to perform circuit imaging -- that is, coding -- in a high level computer language, the DUT logic diagram. Once this phase is completed, the test programmer begins to generate the test program by developing input stimuli to initialize the DUT and exercise its major functions. The simulator aids the programmer by providing complete response information for each node in the circuit. This information provides the test programmer with feedback concerning the effects the input stimuli have on the DUT. Once the programmer is relatively confident his test program has initialized the circuit and exercised all the elements, he "marries" the test program to the physical printed

circuit board. This is to determine whether any problems exist with the test program. Some of the problems which may be encountered are the following:

- o Mistakes in the circuit description/topology
- o Inappropriate input stimuli
- o Incorrect initialization.

Use of a simulator system for test program generation yields many benefits to the user. One of the benefits is that the quality and the fault comprehension of the test program can be gauged by the simulation system. Another benefit is the generation of DUT internal nodal data by the simulation system. This data may be utilized in conjunction with a digital tester and diagnostic probe to provide the test operator with diagnostic information about the DUT. The obvious benefit is that the simulator generates the test program output response.

### 6.3.3 AUTOMATIC TEST PROGRAM GENERATION

Automatic Test Program (ATPG) is the process by which system software automatically generates some or all of the input stimuli required to detect faults in a digital DUT and provides the output response that detect these faults. It also provides the percentage of faults detected (comprehension) and in same cases, lists faults which have not yet been detected. Although the user does not have to generate input patterns, he must thoroughly understand and describe the circuit topology. Usually ATPG systems utilize a simulator to generate the test program and diagnostic information (similar to the simulation technique mentioned earlier).

The ATPG operates by generating input sequences which follow a sensitized path through a logic circuit. A change in logic state in the path causes a variation at the output of the circuit. Consider a path which contains a stuck logic state fault. The stuck fault is considered discovered if a change in logic state in the path fails to propagate to the circuit output. Input stimuli may detect faults which are created along other paths also. By simulating the generated input stimuli, the fault comprehension can be computed.

After a number of sequences are created by the ATPG generator system, their effectiveness is measured by the simulator. On the basis of this information, the user

-etains only the effective patterns. The simulator-based technique is employed to generate the response (output) information. Finally, to determine if it contains any errors, the test program is verified against the digital DUT. If any incompatibility is discovered, the input stimuli and ATPG pattern generator directions are altered.

Some of the disadvantages of ATPG are:

- o Tests cannot be generated for every possible circuit since the IC library can be incomplete particularly for complex IC's.
- o Detailed modeling is required.
- o The user must possess knowledge of the strengths and weaknesses of the system particularly in the case of circuit timing analysis.
- o Large, costly computers may be required.
- o Many computer CPU hours are required to simulate a complex circuit.
- o Diagnostics are generated generally assuming a single fault occurs at a time and no intermittent faults just hard faults.

Some of the advantages of the ATPG are:

- o It is necessary to develop only the circuit image or mode for creation of the test program.
- o It may be effectively used on small and intermediate size SSI and MSI printed circuit boards.
- o It provides consistent results (quality)
- o It reduces/eliminates duplicative test sequences (fault compression).
- o It determines the percentage of faults detected (comprehension) and in some cases, lists faults that are not detected.

### 6.3.4 CONCLUSION

In view of the above discussion, it was concluded that the following four (4) areas are prime targets for ATPG enhancement since they are essential to providing a practical and efficient tool for future test program development for VLSI PCBs.

- IC Library Expansion

The more complete and accurate the IC library the better the ATPGs performance in test program development. This is the most apparent limitation of the ATPG technique, namely, the requirement that all ICs on a given circuit board be modeled. For this purpose a large IC library containing hundreds of ICs is available with any good simulator software.

Elements such as large RAMs, ROMs, ALUs and FIFOs are all found in such libraries. New ICs however need to be modeled, especially custom LSI chips. This is time consuming and may be difficult. This makes IC library expansion of the simulator a necessity and is of prime importance in ATPG's enhancement in order to provide complete and timely support for testing of the complex circuit boards of today and tomorrow.

In addition, there is the problem of successfully modeling microprocessor chips. Can they be modeled practically by ATPG on a minicomputer? Although there have been many different attempts to model microprocessors, it seems that microprocessor models as yet have not been rigorously proven out on a software-simulator system. ATPG's of today and tomorrow need to address and solve this problem for them to be a complete technical and cost effective software tool.

- Improved Timing Analysis

Another difficulty with many existing ATPGs is the unit delay analysis approach. For many current and future technology circuit boards a unit delay simulator is inadequate for the task of programming printed circuit boards that are heavily populated with VLSI devices and are to be tested on a dynamic tester. This particular problem requires worst-case timing analysis to be performed by the simulator. The implementation of such a feature has been provided in a few simulators in the past and most recently in LASAR Version 6.00 and "HIT" ATPG developed for the military by Grumman

Corporation. In LASAR Version 6.00, a high level timing language and associated compiler, generates the data base necessary for accurate timing simulation. The primary advantages of this language are its dual structure and functional timing capabilities. The structural timing feature permits independent delay values to be assigned to each primitive within a device. The structural timing data base produced is appropriate both for chip design verification and for test generation. The functional timing capability is critical especially when the manufacturer's specification sheet is the only source of timing data.

Thus, simulators/ATPGs that incorporate timing analysis capabilities, as LASAR 6.00 and "HIT" , should be investigated to the extent of evaluating their performance regarding their capability to satisfy the circuit analysis requirements of the future technology described in this report.

- Reduction of Simulation Run Time

Presently simulators/ATPGs require many computer CPU hours to simulate complex circuit boards which is both costly and time consuming. Therefore, there is a definite need to investigate ways to reduce computer simulator CPU time for the generation of testing analysis. One possible approach for study is the use of a parallel processing technique for simulation and behavioral analysis and other techniques of artificial intelligence.

The parallel processing may be used to greatly increase speed and efficiency of ATPG simulation in two areas, namely, logic simulation and fault simulation by sharing of computation workload by multi-process cell. with each process cell having its own memory and the ability to communicate with other processor cells. However, when the size of the circuit approaches the limits of the representations capacity of the host computer, the speed advantage disappears. This is where artificial intelligence techniques may provide some solutions. For example, a behavioral (high level) description of a device within a circuit or of a circuit can reduce the problem to a manageable size and greatly increase the speed of the test generation process.

o Improved Diagnostic

The segment of computer science called Artificial Intelligence (AI) which for the most part is in the early stages of development except with reasoning power offers a possible viable approach to improving ATPG diagnostic generation. This is possible because computer programs cannot only approach human performance but can sometimes exceed when dealing with reasoning from knowledge in test programming.

The conventional diagnostic process for test programs is to assume that a single fault occurs at a time. However, in reality, multiple and intermittent faults can occur. The conventional diagnostic approach has difficulty with the latter situation because it uses the circuit topology and the failed pin to guide the diagnostic search for the fault. It also uses a hierarchial search method which depends on limited test point access. Therefore, in cases where there is no access to perform a required test for program fault isolation, the program must proceed as far as possible on the basis of incomplete or partial information, often resorting to alternative types of knowledge, such as component failure rates.

An AI enhanced ATPG would differ from a conventional ATPG in the following way. The conventional ATPG uses a straightforward algorithm approach that entwines the pertinent knowledge of the problem and the method for using the knowledge. The AI enhanced ATPG would generate test program that use a heuristic approach with a clever separation of general knowledge about the problem and the method for applying the general knowledge ot the problem. With this separation of knowledge and method, the program could be modified by a simple change in the knowledge data base.

Thus, during test program development, such AI enhanced ATPG program could be modified by accessing knowledge data base (hypothesis) and using operator interaction. A hypothesis generator (inference system) would be responsible for the reasoning, creating and refining hypotheses to account for the outcome of the diagnostic tests. The hypothesis generator using a

heuristic approach would draw on the knowledge data base that would include such information as: user's own primitive, non-gate level stuck at faults and multi-fault model alternatives, predetermined fault analysis data and historical data on the PCB circuits and components.

The choice among competing hypotheses is narrowed down to one hypothesis based on the outcome of diagnostic tests. However, it is quite common for the hypothesis generator to find more than one hypothesis that could account for a given diagnostic test result. To handle this, it enters a special choice protocol mode in which it attempts to find evidence for and against each candidate. If the evidence is not already available, the hypothesis generator runs additional tests that seem most likely to produce the evidence. If no additional testing appears profitable, it will favor the hypothesis with the most findings and will proceed to refine each element of the hypothesis.

Finally, an interaction mode is invoked if the hypothesis generator needs to receive information that is not yet in the data base and cannot be deduced in any other way by asking the user.

When a terminal hypothesis has been reached, a repair operation is requested for DUT. After the repair action, a termination test is run to determine if all faults have been isolated and repaired. If yes, the diagnostic search ends. Otherwise, the search for multiple failure resumes with the most refined hypothesis which is more general then the current terminal hypothesis and which was not affected by any piece of evidence to be revoked as a result of the most recent repair operation.

### 6.3.5 RECOMMENDATION

In order to improve ATPG simulation times and diagnostic analytic capabilities, it is recommended that the Army investigate/study the possibility of marrying ATPG algorithm system with artificial intelligence and parallel processing techniques.

# APPENDIX A

# ATPG SELECTION CONSIDERATIONS

## A.1 GENERAL SELECTION CONSIDERATIONS

### A.1.1 IMPLEMENTATION LANGUAGE

In evaluating different ATPGs the user should select one in which the ATPG software is implemented in a high order programming language (HOL) of widespread availability. This feature provides the user with system portability, that is, the ability to transport the software to run on a different computer without a vast amount of software re-coding effort. However, the specifics of the language should be scrutinized before it is assumed that the software is transportable. Typically the programming language for ATPGs is FORTRAN or Assembly or a combination of the two. Using a HOL such as FORTRAN provides for efficient, cost-effective software implementation. However, in order to allow for optimum performance, it may be beneficial to have key subroutines written in Assembly language.

### A.1.2 HOST COMPUTER

The computer system on which the ATPG software operates should be a commercially available computer system. These computers typically range from a 12-bit PDP 8 minicomputer (or a functionally compatible system) to a CDC series 6000 main frame system. The computer system selected should be available for a minimum of 10 years.

Simulation and test generation for complex digital DUTs are inherently memory intensive. Thus, a memory expansion capability to at least 4 megabytes of directly addressable memory is advisable for the system selected.

### A.1.3 OPERATING MODE

The user selecting an ATPG system must also consider the hardware/software setup of the system. The operating modes usually available consist of interactive for minicomputers and timeshared systems and batch for most main frame setups. Both modes have advantages and disadvantages. The batch mode allows the user to specify in advance all information necessary for running any function of the ATPG system, so that it can be executed later in the user's absence.

However, if the ATPG is used as an interactive test program generation tool (rather than as an ATG tool), an interactive mode with display capability is of utmost importance.

### A.1.4 SYSTEM AVAILABILITY

The simulator/ATPG system's availability and the applicability of a simulator to a specific ATE play and important role in the selection process.

Most simulation systems provide the GO/NO-GO test program as an output and do not generate the probe diagnostic data or fault dictionary data in a format acceptable to the tester. Because this fact alone can determine the applicability of a simulator, it is important to exemplify the problem. Assume the application is to develop test programs with the simulation outputs used on GenRad 1792 test system. Clearly, GenRad CAPS VIII software should be considered as a simulator selection which provides complete test data for the GenRad tester consisting of:

- The GO/NO-GO test program.
- The probe circuit file.
- The IC nodal data.

Assume now that the simulation system "x" is preferable because it is already available to the user and has additional capabilities such as internal IC faulting and timing analysis. This, however, may cause a problem because system "x" provides a GO/NO-GO test program to the GENRAD test system but does not provide probe data. In this situation the user has two choices:

- Use CAPS VIII and sacrifice the additional capabilties available in system "x".

or

- Use system "x" first and generate a GO/NO-GO test program for CAPS VIII. Next, generate a CAPS VIII circuit file and re-simulate the DUT on CAPS VIII using the GO/NO-GO test program generated by system "x" as an input

stimulus. CAPS VIII will now generate all probe diagnostic data. Finally, the user must compare the CAPS VIII simulation data with system "x" simulation data to assure correctness.

Given such serious interfacing problems, even the best simulator may be less desirable than the one available with the test system.

### A.1.5 DESIGN FOR TESTABILITY

The testability of a Device Under Test (DUT) will have a major impact on whether a simulator can be used effectively to model a circuit and on the cost associated with using a simulator to develop a test program.

As for easy test program generation, circuit topology and size play an important role. Though many test program generation algorithms, such as D-algorithm, have been developed, almost all of them are primarily intended for combinational circuits. While test programs for combinational circuits have been effectively generated by using such algorithms, it is much more difficult to apply these algorithms to sequential circuits. Several automatic test program generators for medium sized sequential circuits have been developed. "owever, sufficiently effective ones for large sized circuits are not yet available.

Another important factor which will affect test program generation cost is circuit size. Today, circuit elements included in LSI chips/cards are increasing rapidly. It is ManTech's experience that the cost to generate test programs will increase in proportion to the square of the circuit size. If the circuit can be partitioned into several sub-circuits logically and test programs can be generated for each of them independently, the total cost for the whole circuit can be reduced to $a/n^2$ (here "n" indicates the number of sub-circuits and "a" indicates overlap ratio). When overlap ratio "a" can be kept within a reasonable range, circuit partitioning also contributes to test generation cost reduction.

| | Size | Cost |
|---|---|---|
| Original Cost | 1 | 1 |
| Sub-circuit | a/n | $(a/n)^2$ |
| Expanded Circuit | a | $a^2/n$ |

## A.2 DETAILED ATPG SELECTION CRITERIA

An approach used in selecting the guidelines is to focus on the simulator's capability to simulate or model the DUT circuitry. It is this aspect of the simulator that is being addressed in the selection criteria.

### A.2.1 IC MODELING

#### A.2.1.1 IC Modeling Techniques

One of the main factors affecting IC Modeling is the technique which generates IC models. For some simulation systems such as CAPS and LOGCAP, the test programmer can take the logic diagram of an IC from the manufacturer's catalog and immediately describe it as a regular circuit to the system. The process is simple and the result is accurate. For other systems such as FLASH, the programmer may have to write a FORTRAN program for the IC, requiring him to transform the logic diagram of the IC into a flow chart so that the FORTRAN routine can be written. This is a difficult and error-prone task.

Another important characteristic in IC modeling is the attainable circuit complexity of an IC. For systems such as FAIRTEST, ICs are modeled only with gates, often making it impractical to model large chips (e.g., RAMs, ROMs, etc.). Most other simulators use functional blocks to model ICs ("functional model") in which the complexity of the functional blocks varies from simple flip-flops to complex LSI chips. A few systems have recently been augmented with special LSI modeling languages (CAI Simulator, CAPS, and MICROSIM) to allow complex LSI chips to be modeled as single, very large functional blocks.

A third major consideration is the availability, quality, and size of the system's IC library ranging typically from 10 to 100 unique models for LOGCAP and DFA to 800 unique models for GRASS. Vendors advertise much larger libraries (over 1,000 ICs) because the total number of IC names (7400., 74L00, etc.) in a library is often as much as four times larger than the number of unique models, due to the functional equivalency of ICs.

— Gate Level

The simulation system shall contain a library of Boolean primitives.

A primitive element is a basic logic device for which the simulator has a specific subroutine to evaluate the response of the element, i.e., determine the outputs and new internal states given the inputs and previous internal states. It is required that the ATPG system provide standard Boolean (gate-type) devices as primitive elements. This includes, but is not limited to, NANDs, NORs, ANDs, ORs, XORs, XNORs, buffers, inverters, and tri-state buffers. Furthermore, these devices must accept an arbitrary number of inputs with a range of 1 to n, where n is a maximum of 16.

— Functional

The simulation system shall have a library of functional primitives.

A functional primitive is a more complex (than a gate) logic device. The ATPG system must provide, as a basis, numerous functional primitives including but not limited to encoders, decoders, selectors, latches, flip-flops (JK master slave, D edge triggered), multivibrators, adders, shift registers, counters (synchronous and asynchronous), read-only memories (ROMs) and random access memories (RAMs).

### A.2.1.2 IC Library

There will be multiple IC libraries, initially containing at least 200 unique models from the SN7400 series of devices.

The initial ATPG system must provide a main system library which includes as a minimum 200 unique models from the SN7400 (Texas Instruments designations) series of devices. Where possible, both a gate level and a functional level model will be

provided. In addition to the model information, (i.e., the data needed for simulation), the library entry for each IC must include supporting data, such as that needed for computer-guided probing, including voltage threshold information, connectivity data, and delay times. Finally, each IC entry will contain the date the entry was last modified.

### A.2.2 CIRCUIT MODELING

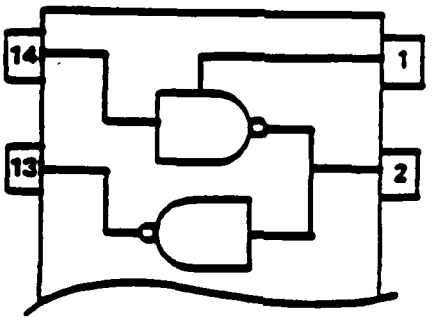
One of the main factors affecting circuit modeling capability is the circuit complexity that the simulation system can model. The circuit complexity can be quantified by considering the gate population and the node count.

The gate population which represents the size of a circuit can be measured by an "equivalent gate count", i.e., a circuit is exploded into AND, NAND, NOR and OR gates and the count of all gates determines the circuit size. The advantage of this measure is that it differentiates between circuits with the same number of ICs, but with vastly different complexities. For example, an average 100 IC circuit with several large LSI chips may be equivalent to as many as 50,000 gates.

The node count is the maximum number of nodes a system can model. Most of the systems can model internal IC nodes or external nodes. Which of the two is used is dependent upon the level of fault isolation required. If fault isolation of internal gates to the IC is required, then internal node modeling is necessary. If fault isolation to the IC is required, then external node modeling will suffice.

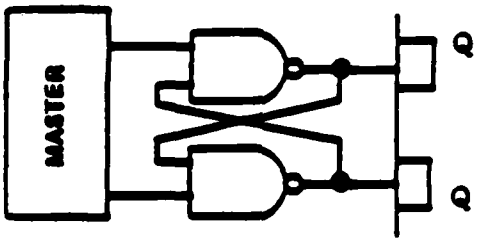
Another important characteristic in circuit modeling is whether the user must concern himself with wired-AND/wired-OR nodes. A wired-AND node is formed by two outputs, which when tied together generate a logic value equal to the logic "AND" of the two output values. A wired-OR node assimilates the value of the logic "OR" of the two outputs. That is, the circuit processor automatically recognized the condition of outputs (buses) being tied together and inserts the appropriate AND/OR gate. For the other systems, the user must recognize the conditions and modify the circuit with the additions of special AND/OR gates in place of the wired nodes.

A fourth major consideration is whether or not the user must concern himself with buses. Few systems handle IC bus conditions automatically. An IC bus pin exists whenever the pin can be used as both a driver and receiver. For example, pin number 2 of the IC below is a bus:




IC BUS PIN

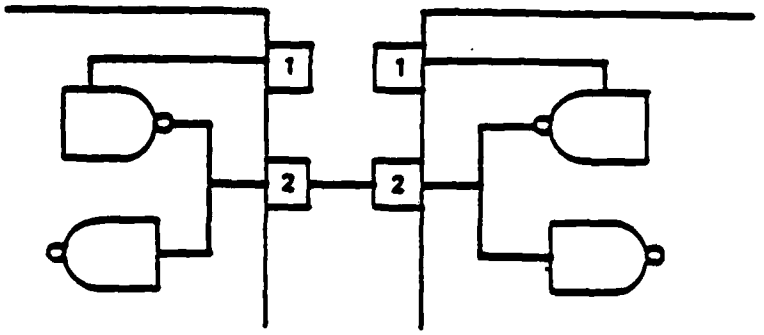
Pin number 1 (tri-state control) and pin number 14 are inputs; pin number 13 is an output. A less obvious bus condition exists at the outputs of many flip-flops whenever *their output latch is unbuffered:*



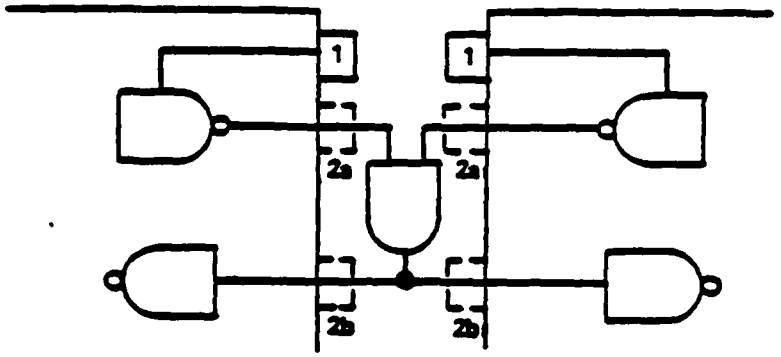

MASTER SLAVE FLIP-FLOP

While it is unlikely that another driver would be attached to the Q line of a flip-flop, the pin nevertheless is a bus because a second drive such as a stuck fault does affect other functions of the IC, such as the Q pin in this case.

For systems which do not support bus pins, the user must model the IC with two pins for every bus pin, one as an input and the other as an output. A typical wired-AND condition for this work-around solution if shown below:




ACTUAL CIRCUIT




WORK-AROUND MODEL

If an IC bus pin is used only as an IC output pin, the user must concern himself only with the stuck condition at such a pin. Several systems which do not deal with bus pins have a special provision for stuck faults at the outputs (buses) of flip-flops and counters. In particular, these elements are implemented as one functional block and the system looks for the presence of stuck faults at their output pins in order to compute the next state.

- Gate Population

  The simulation system's software architecture shall be capable of accommodating circuits containing at least 65,000 equivalent gates.

  Although it may not be the case that an actual circuit of this many gates can be simulated by a particular ATPG system hardware configuration, the basic ATPG system must be designed so that no software limitation lower than 65,000 exists on the number of equivalent gates.

- Node Count

  The software architecture must be such that at least 65,000 circuit nodes can be accommodated.

  Although it may not be the case that an actual circuit of this many nodes can be simulated by a particular ATPG system hardware configuration, the basic ATPG system must be designed so that no software limitation lower than 65,000 exists on the number of circuit nodes.

- Automated Handling of Wired "AND"/Wired "OR" Nodes and Buses

  There will be a capability to handle bi-directional pins, buses, and wired-AND/ORS automatically.

  Bi-directional pins on the circuit device (e.g., IC) level must not require any special identification or handling in the circuit description. These pins must be recognized as such by the circuit processor (from the information in the library data base) and any special structures required, such as additional or diplicate IC pins, must be automatically generated by the circuit processor. Similarly, bus nodes and wired-AND/OR functions must also require no special handling (or even recognition) by the user in the circuit description. The circuit processor must automatically recognize these conditions and again provide whatever special structure is required by the simulators. When these conditions occur, they must be reported to the user.

## A.2.3 CIRCUIT SIMULATION

The main factor affecting good circuit simulation is the simulation accuracy, which is dependent on the number of logic states and the parameters associated with modeling logic timing.

Most simulators model 3 logic states (logic 0, logic 1, unknown = X) and use a "unit delay" timing model, e.g., each device in the circuit has a logic delay of one. For static testing, this simulation accuracy is sufficient as proven by the use of various commercial test systems such as CAI Simulator, CAPS, and TESTAID III. Testers have been linked to these "three valued logic" unit delay simulators and the simulation data have been successfully applied to the testing and diagnosing of millions of boards.

For certain applications, a higher simulation accuracy is desirable requiring either more logic states or better timing accuracy. For example, for tri-state, bus-structured logic the user may want to simulate the "high impedance" state in addition to the other three states (0, 1, X). For CAD, a simulator with a timing analysis capability is very valuable. A test program generation system such as TEGAS III with this added feature may be the most applicable one.

- Logic States

  As a minimum, the simulator must simulate 4 logic states (0, 1, X, Z).

  In addition to the standard logic states of 0 and 1, the simulator must handle the indeterminate state (X). This state represents an uninitialized or otherwise indeterminate logic value. Also, the high impedance state (Z) must be handled by the simulator. This state represents electrical disconnection which is common on bus-structured devices. The simulator must automatically report to the user the condition which occurs when more than one device is found to be active on the bus (i.e., bus contention). Floating (high impedance) inputs must be correctly interpreted by the simulator, depending on the technology of the devices being simulated.

- Logic Timing Model

  The simulator must as a minimum simulate one nominal, inherent delay for each device output.

  Each device (primitive) output must have associated with it one delay, representing the nominal (typical) delay for a transition from the input of the device to its output. The delay will be initially specified in the IC library, but may be overridden by the user at circuit processing time. Note that the delay must be simulated as inherent delay; i.e., a pulse smaller than the inertial delay will be filtered out by the simulation process. The capability must be provided to specify these delays with a resolution of up to 1 nanosecond.

### A.2.4 FAULT SIMULATION

Factors which impact fault simulation capability include fault modeling capabilities. All simulators analyze for the standard input and output stuck-at-0 and stuck-at-1 faults at the IC pin level. For certain applications, such as manufacturing, this may be insufficient and the additional capability to analyze internal IC faults is required. For situations where the fault diagnosis is based on a fault dictionary, manufacturing faults such as shorts between tracks and adjacent IC pins should be simulated for inclusion into the dictionary. There are several simulation systems that offer these capabilities, e.g., FAST, LOGOS, CAPS.

Another important characteristic in fault simulation is a list of detected and undetected faults. The availability of fault dictionary output from the fault simulator is also a consideration. The types of fault dictionaries include first detect, n-detect, and "up to complete isolation". A fault dictionary contains fault signatures for each of the faults simulated and detected by the system. In a first detect dictionary, the only data kept for each fault are the erroneous external output responses at the first failing step. With this type of dictionary, there are liable to be many faults which have identical dictionary entries (signature). Thus, a physical DUT which exhibits a failing response will often be matched with many possible failures, i.e., the diagnostic resolution will be low. In order to improve the diagnostic resolution, many systems store a user-selectable number (n) of failing responses for each fault, increasing the likelihood of unique

signatures. Finally, LOGOS III and D4-LASAR automatically store as many failing responses as are necessary to isolate failures. However, topological considerations as well as the nature of the test program may prevent good fault resolution from being attained in all cases. A method to overcome this last problem is D4-LASAR's ISO-PROBE. It increases the resolution of the fault dictionary by requesting the operator to probe certain nodes in order to isolate a fault to a single IC. In essence, the probe operates as an extension to the edge connector with a signature derived from the edge connector and the probed pins.

It is important to note that storage requirements may become so large with the n-detect and "complete" fault dictionaries that they overextend system capacity. Therefore, fault resolution requirements must be balanced with storage availability, the cost of dictionary generation, and retrieval time.

The term "X-detection" in the matrix refers to dictionary entries created for "potentially" detected faults, i.e., those that are detected by an unknown condition propagating to a primary output which has a known value in the good circuit. Some systems have extensive algorithms to deal with such fault conditions.

In addition the simulation system should provide fault resolution information. This information shows the degree of fault isolation which is attained by the fault dictionary. It is also a useful measure in specifying the number of components which must be replaced in order to correct the fault as identified by the fault dictionary.

- o <u>Fault Types</u>

  The following fault types selectable by the user must be analyzed by the fault simulator:

  (a) IC outputs stuck-at-0 and stuck-at-1
  (b) IC inputs stuck-at-0 and stuck-at-1
  (c) Primitive outputs stuck-at-0 and stuck-at-1
  (d) Primitive inputs stuck-at-0 and stuck-at-1.

  In the stuck-at fault model, an individual lead in the circuit is assumed to become permanently fixed at the logical 0 or logical 1 level. It is necessary

to distinguish between an input stuck and an output stuck. An input stuck is defined as affecting only the input of the IC or primitive device in question. However, an output stuck affects all ICs or primitive devices on a given circuit node (all those connected to the output of the IC or primitive device in question).

- Fault List

The fault simulator must provide a list of detected and undetected faults.

The list of detected and undetected faults will identify by name the node and type of fault which was considered. For all detected faults the list must include the test step number at which the fault was detected for the first time.

- Fault Dictionary

The ATPG system must provide a fault dictionary output.

For the purposes of automatic fault isolation, the ATPG system must provide a fault dictionary as a user-selectable post-process to fault simulation. This file must be a binary representation of the fault signatures for each fault simulated. Due to the fact that all these signatures can consist of a very substantial amount of data, they must be optimized to conserve (disk) storage. Also for this reason, the extensiveness of the dictionary must be specifiable by the user in several regards (via control commands). First of all, the fault dictionary may include only the signature of the first failing test for each fault, it may include the signatures of the first n (where n is specified by the user) failing tests, or it may include the signatures for all failing tests.

In addition to the fault dictionary itself, a module must exist to print out the dictionary in a user-oriented format, providing for manual lookup. In particular, the printout must be organized in such a way that, given a signature, the user can quickly locate the fault or faults which produce that signature.

- Fault Detection

  There must exist a capability to sample a percentage of all faults for fault analysis to statistically determine fault detection.

  Under this user capability, a sample of the total number of faults considered will be selected at random by the ATPG system for simulation. The percentage of faults considered will be selectable by the user. Using this random sampling, the ATPG system can statistically determine, with a known confidence factor, the percentage detection of all faults under consideration. Under this option, the system will provide the list of sampled faults, the percentage detection of those faults, and an indication of whether each faults was detected and at what step it was detected.

### A.2.5 AUTOMATIC VECTOR GENERATION

The final technical capability consideration is automatic test generation (ATG). The main consideration in evaluating vector generators is the generation strategy employed by the system. The simplest technique is to generate random numbers between 0 and $2^n$ where n is the number of the input vector bits (edge pins) of the DUT. Clearly this technique has little value for all but combinational circuits and should be rated very low. It is possible to augment this technique by applying bias factors to each bit position in the vector and to increase occurence probability of certain random numbers and totally eliminate others.

The most successful vector generation techniques are based on a path sensitization strategy in which a sequence of vectors is generated for a specific fault (or faults) by activating that fault and sensitizing a path from it to the edge of the connector. This vector generation algorithm is frequently combined with heuristic techniques which provide guidance to path selection strategy. D4-LASAR, LOGOS III, and INDICATES are the most advanced and successful of these systems.

The vector generators described above create "arbitrary" input stimuli by activating and sensitizing faults rather than exercising the circuit in accordance with its function. This arbitrariness causes race and hazard problems in the logic of the circuit.

Thus, it is important that the ATG system offers a capability to eliminate or avoid these logic timing problems. D4-LASAR and INDICATES offer a race and timing analysis program which flags races and automatically changes the input stimulus in order to "derace" the pattern. Other systems such as LOGOS, FAIRTEST, FANSIM, of CAI's vector generator have built-in heuristics which guide the vector generation strategy to avoid race laden patterns.

Two other feature were also factored into the rating of ATG systems, namely, the user control capabilities and special circuit limitations.

Efficient use of the vector generation system requires detection of various interactive system control features such as:

- o The capability to mix manual and automatic patterns
- o The capability to stop the vector generation scheme if the test sequences are too long, the detection percentage per test step is too low, etc.
- o The capability to stop the vector generation strategy if a CPU time limit is exceeded.

Finally, automatic vector generation is likely to restrict the circuit complexity beyond the limitations imposed by the simulation systems. These restrictions involve both overall gate count and specific circuits such as counters, shift-registers, one-shots, pulse circuits, RAMS, etc.

- o <u>Vector Generation</u>

  A capability to automatically generate input stimuli vectors must be provided in the system.

  This capability, commonly referred to in the the industry as ATG or Automatic Test Generation, provides for automatic input stimulus pattern generation by performing an analysis of the circuit model entered into the system.

The ATG algorithm shall be capable of generating input patterns for both combinational and sequential circuits, and shall have the capability to initialize sequential circuits.

- o Mix Manual and ATPG

The ATPGs shall have capability to intermix patterns which have been interactively and/or manually generated with those that are automatically generated by the system.

In addition, the ATG algorithm will be such that it does not attempt to generate patterns to detect faults which have already been detected by previous patterns, regardless of how those previous patterns were generated.

- o Control Capabilties

It shall be possible for the system to stop generating patterns automatically based on both:

- — A user set level of fault detection being achieved, or
- — A user set limit of computer time being reached, whichever occurs first.

# APPENDIX B

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# APPENDIX C

# ACRONYMS AND ABBREVIATIONS

| | |
|---|---|
| ADC | Analog To Digital Converter |
| ALU | Arithmetic Logic Unit |
| ATE | Automatic Test Equipment |
| | |
| Baud | Binary Units of Information Per Second |
| BIT | Built-in Test |
| BITE | Built-in Test Equipment |
| Bits | Binary Digits |
| bps | Bits per Second |
| Byte | A group of eight (8) binary digits |
| | |
| CMOS | Complementary Metal Oxide Semiconductor |
| CMOS/SOS | Complementary Metal Oxide Semiconductor/Silicon-on-Sapphire |
| CPU | Central Processing Unit |
| | |
| DFT | Design for Testability |
| DRAM | Dynamic Random Access Memory |
| DUT | Device Under Test |
| | |
| EAROM | Electrically Alterable Read Only Memory |
| ECL | Emitter-Coupled Logic |
| Est. | Estimated |
| | |
| FIFO | First In First Out |
| | |
| GaAs | Gallium - Arsenide |
| | |
| HMOS | High Performance Metal Oxide Semiconductor |
| HOL | High Order Programming Language |
| HTL | High Threshold Logic |
| | |
| IC | Integrated circuit |
| $I^2L$ | Integrated Injection Logic |
| ISL | Integrated Schottky Logic |
| | |
| K | Kilo or Thousand |
| Kb/s | Kilobits per second |
| KIPS | Kilo-instruction per Second |
| | |
| LRU | Line Replaceable Unit |
| LSI | Large Scale Integration |
| $LPST^2L$ | Low Power Schottky Transistor - Transistor Logic |
| | |
| M | Mega or Million |
| ma | Milli-ampere |
| Mb/s | Megabits per Second |
| MCF | Military Computer Family |
| MIPS | Million Instruction per Second |
| MP | Microprocessor |
| MSI | Medium Scale Integration |
| MLRS | Multiple Launch Rocket System |
| MOS | Metal Oxide Semiconductor |

| | |
|---|---|
| mSec | Milli-second |
| MTBS | Mean-Time-Between-Failures |
| mv | Milli-volt |
| N/A | Not Applicable |
| NMOS | N-Type Metal Oxide Semiconductor |
| NRZ | Non-return to Zero |
| N/S | Not Specified |
| nSec | Nanosecond |
| NTDS | Naval Tactical Data Systems |
| PCB | Printed Circuit Board |
| PMOS | P-Channel Metal Oxide Semiconductor |
| PROM | Programmable Read-Only Memory |
| RAM | Random Access Memory |
| Resp | Response |
| ROM | Read-Only Memory |
| RZ | Return to Zero |
| SEC | Second |
| SSI | Small Scale Integration |
| Stim | Stimulus |
| STL | Schottky Transistor Logic |
| TTL | Transistor-Transister Logic |
| uSec | Microsecond |
| UART | Universal Asynchronous Receiver Transmitter |
| V | Volts |
| VLSI | Very Large Scale Integration |